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[54] **METHOD OF MAKING METAL-INSULATOR-METAL JUNCTION STRUCTURES WITH ADJUSTABLE BARRIER HEIGHTS**

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[58] **Field of Search** ..... 437/175, 176, 177, 178, 437/179; 357/6, 7, 15; 148/DIG. 139, DIG. 140, DIG. 142

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,056,073	9/1962	Mead	317/234
3,448,350	6/1969	Yamashita et al.	317/234
3,702,956	11/1972	Benard et al.	317/234
3,938,243	2/1976	Rosvold	148/DIG. 139
4,107,724	8/1978	Ralph	357/7
4,163,677	8/1979	Carlson et al.	357/15
4,220,959	9/1980	Kroger	357/5
4,371,884	2/1983	Esaki et al.	357/12
4,377,031	3/1983	Goto et al.	437/175
4,421,577	12/1983	Spicer	437/176
4,449,140	5/1984	Board	357/7
4,490,733	12/1984	Kroger	357/5
4,638,342	1/1987	Freeouf et al.	357/15
4,763,176	8/1988	Ito	357/15
4,946,803	8/1990	Ellwenger	437/177

OTHER PUBLICATIONS

"Polycrystalline Semiconductor Solar Cell", IBM TDB vol. 17, #8 Jan. 1975 p. 2455.

"Control of Silicon Content in Schottky Barrier Diode Metallurgy", Giddings et al., *IBM Tech. Discl. Bul.* vol. 16 No. 2 Jul. 73 pp. 615-616.

"Minority Carrier Confinement Thin Film Solar Cell", Hovel et al., *IBM Tech. Discl. Bul.* vol. 18 No. 2 Jul. 75 pp. 544-545.

"Metal-InAs Contact for Vertical Heterojunction Transistors", Jackson et al. *IBM Tech. Discl. Bul.* vol. 29 No. 5 Oct. 86 pp. 2235-2236.

(List continued on next page.)

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[57] **ABSTRACT**

A method and structures are described for fabricating junctions having metal electrodes separated by polycrystalline barriers with arbitrarily-chosen but controlled barrier height and shape is accomplished by varying the composition and doping of polycrystalline multinary compound semiconductor materials in the barrier, hence varying the Fermi level pinning position such that the Fermi level is fixed and controlled at and everywhere in between the two metal-insulator interfaces. It is known that Schottky barrier heights at metal/compound semiconductor interfaces are determined by a Fermi level pinning mechanism rather than by the electronic properties of the applied metallurgy. The present invention exploits the knowledge that the same type of Fermi level pinning occurs at semiconductor dislocations and grain boundaries. The present invention uses polycrystalline compound semiconductor alloys in which the pinning position is varied over a large range in metal/semiconductor structures. The structures are composed of sandwiches of metal, compound semiconductor and metal. Tunneling currents are determined by barrier height, controlled by semiconductor alloy composition, and semiconductor thickness. The energy barrier in the polycrystalline material can be uniform throughout, due to the uniformity of pinning position at both the metal/semiconductor interface and the grain boundaries.

8 Claims, 5 Drawing Sheets